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DESIGN AND ANALYSIS OF VOLTAGE COMPENSATION TYPE OF ACTIVE SUPERCONDUCTING FAULT CURRENT LIMITER

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Abstract— This paper presents the operation principle of voltage compensation type active superconducting fault current limiter (SFCL) for the three phase power transmission system. A voltage compensation type active super-conducting fault current limiter is composed for three phase air core super-conducting transformer & PWM converter. The primary winding of three phase air-core super-conducting transformer is connected series with the AC main circuit & secondary winding connected in star with the super-conducting coil through a PWM converter. In normal condition, the effect of SFCL on transmission line voltage level is minimized with the help of external source such as PWM converter. During the short circuit state, fault current level is minimized by controlling the impedance of primary winding, amplitude of current and phase angle. Those parameters of SFCL design to meet the system requirement further using a MATLAB SIMULINK. We can analyzed voltage compensation type active superconducting fault current limiter can operate easily. The new model of active SFCL is developed & simulation succeed this SFCL can suppress with the fault current effectively.

Keywords—PWM- Pulse width modulation, SFCL-superconducting fault current limiter.

I. INTRODUCTION

In our country due to continual development demand of electricity is increases, electricity network is expand and the level of fault current increases and it is hazards to the power system network. It is need to maintain fault current at minimum level and reduce the over current effect on electrical equipments. Solution for that one device is to be developed that is SFCL, With the help of this device we can reduce the electro-mechanical forces, fault current level and heating problems system make healthy condition with in little time. This superconducting fault current limiter has influence on the power system network. This super conducting coil have own impedance, due to that impedance it cause voltage drop and it gives effect on transmission line. Then efficiency of transmission line reduced and it produces impact. This super conducting fault current limiter coil placed in series to the line this coil is called as primary coil of transformer. There we installed a three phase transformer have made up from super

conducting coil and Secondary coil of superconducting transformer is connected through external source to PWM converter [1].

This device technique is associated with the flexible AC transmission system (FACTS), such as series active filter which is part of power electronic. Some study related superconducting material and property of SFCL is carried out with the reference [3].

In this paper provided a solution how to reduce voltage drop and increases efficiency of transmission line, by providing series voltage compensation method. Some additional studies related superconducting materials well as power electronic device, for the application of AC transmission technique use has been done [3-4]. We connect a three phase superconducting transformer in series with the transmission line through the external source such as PWM Converter. This control scheme provided to this superconducting fault current limiter for voltage as well as current level management. We have developed a voltage compensation type active superconducting fault current limiter. Simulation is done in MATLAB SIMULINK & simulation results are succeeded in MATLAB.

II. PRINCIPLE AND STURCTURE OF THE ACTIVE SFCL

From Fig. 1, it indicates the structure of the integrated 3-Phase voltage compensation type active SFCL, which is composition of three air-core superconducting transformers and a three phase four-wire voltage-type PWM converter consisting of full controlled power electronic devices.

L_{s1}, L_{s2} are the self-inductance of the super-conducting windings, and M_s is the mutual inductance. Z_1 is the circuit impedance and Z_2 is the load impedance. L_d and C_d are used for eliminate the harmonics produced by the PWM converter.

In normal state, the injected current in the secondary winding of the each phase superconducting transformer will be controlled to keep a certain value, where the magnetic field in the air-core can be compensated to zero, so the active SFCL will have no influence on the main circuit. When the fault is detected, the injected currents (I_r, I_y, I_b) corresponding to the

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fault phase will be adjusted in amplitude or phase angle, so as to control the superconducting transformer's primary voltage which is in series with the main circuit, and further the fault current can be reduced.

Taking phase R for an example to understand the regulating mode in detail. In normal state, Eq. (1) can be written as:

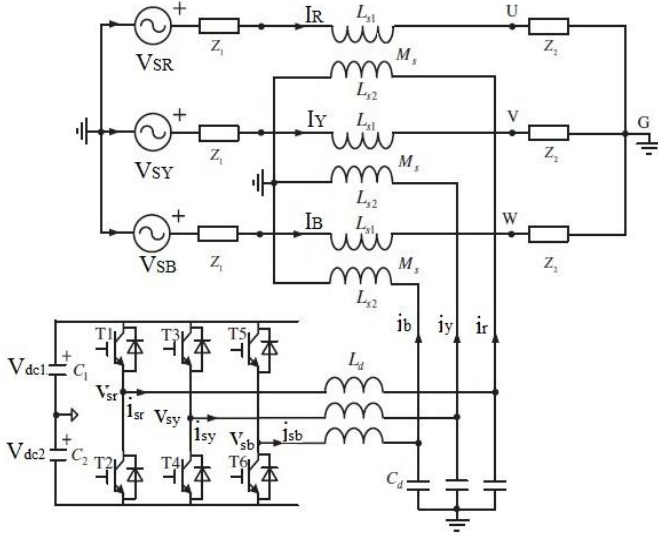


Fig-1. Structure of the three-phase voltage compensation type active SFCL

$$V_{SR} = I_R(Z_1 + Z_2) + j\omega L_{S1}I_R - j\omega M_S I_r \quad (1)$$

Controlling to I_R make $j\omega L_{S1}I_R - j\omega M_S I_r = 0$ and the R-phase superconducting transformer primary voltage V_R will be composed to zero. Thereby, the SFCL will have no influence on R-phase, and I_r can be set as:

$$I_r = \frac{I_R L_{S1}}{M_S} = \frac{I_R \sqrt{L_{S1}/L_{S2}}}{K} = \frac{V_{SR} \sqrt{L_{S1}/L_{S2}}}{(Z_1 + Z_2)K} \quad (2)$$

K - is the coupling coefficient and it can be shown as;

$$K = M_S \sqrt{L_{S1}L_{S2}}$$

When the node V is grounded and the single-phase fault happens, the line current will rise from I_R to I_{Rf} , and the primary and secondary voltages of the R-phase superconducting transformer will increased to V_{SRf} and V_{Rf} , respectively.

$$I_{Rf} = \frac{V_{SR} + j\omega M_S I_r}{Z_1 + j\omega L_{S1}} \quad (3)$$

$$V_{Rf} = j\omega L_{S1}I_{Rf} - j\omega M_S I_r = \frac{V_{SR}(j\omega L_{S1}) - Z_1 j\omega M_S I_r}{Z_1 + j\omega L_{S1}} \quad (4)$$

$$V_{rf} = j\omega L_{S2}I_r - j\omega M_S I_{Rf}$$

$$V_{rf} = j\omega L_{S2}I_r - j\omega M_S \frac{V_{SR} + j\omega M_S I_r}{Z_1 + j\omega L_{S1}} \quad (5)$$

From Eq. (4), the primary voltage can be maintained by regulating I_r , and the superconducting fault current-limiting impedance Z_{SFCL} can be adjusted in the following equation:

$$Z_{SFCL} = \frac{V_{Rf}}{I_{Rf}} = j\omega L_{S1} - \frac{j\omega M_S I_r (Z_1 + j\omega L_{S1})}{V_{SR} + j\omega M_S I_r} \quad (6)$$

According to the different regulating mode of I_r , There are three operation modes:

(1) Making I_r remain the original state, and

$$Z_{SFCL-1} = \frac{Z_2(j\omega L_{S1})}{(Z_1 + Z_2 + j\omega L_{S1})}$$

(2) Controlling I_r to zero, and

$$Z_{SFCL-2} = j\omega L_{S1}$$

(3) Regulating the phase angle of I_r to make the angle difference between V_{SR} and $j\omega M_S I_r$ be 180° . By setting $j\omega M_S I_r = -cV_{SR}$, and

$$Z_{SFCL-3} = \frac{c}{1-c} Z_1 + \frac{1}{1-c} j\omega L_{S1}$$

The air-core superconducting transformer has many advantages, Such as absence of iron losses and magnetic saturation, and it has more possibility of reduction in size and weight than the Conventional transformer and iron-core superconducting transformer [9]. As there is no existence of transformer saturation in the air-core superconducting transformer, adopting it can contribute to keep the linearity of Z_{SFCL} . However, since the air-core superconducting transformer has no specific path for the magnetic flux, the magnetic flux produced by its windings will act directly on each turn of the superconducting winding [10], and the ac losses of the superconducting windings will increase to a certain extent. Besides, the transformer's stability may be affected adversely.

III. PWM CONVERTER CONTROL STRATEGY.

From the analysis of current-limiting characteristics of the integrated active SFCL, it is needed to control the three-phase four-wire PWM converter flexibly and reasonably. Assuming that the switching devices are ideal and the split DC link capacitances are the same ($C_1 = C_2$), according to Fig. 1, the current and voltage equations can be achieved.

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$$\begin{cases} L_d \frac{dI_{Sr}}{dt} + RI_{Sr} = -V_r + V_{Sr} \\ L_d \frac{dI_{Sy}}{dt} + RI_{Sy} = -V_y + V_{Sy} \\ L_d \frac{dI_{Sb}}{dt} + RI_{Sb} = -V_b + V_{Sb} \end{cases} \quad (7)$$

R- denotes the equivalent resistance of L_d .

$$\begin{cases} C_d \frac{dV_r}{dt} = I_{Sr} - I_r \\ C_d \frac{dV_y}{dt} = I_{Sy} - I_y \\ C_d \frac{dV_b}{dt} = I_{Sb} - I_b \end{cases} \quad (8)$$

Further, the mathematical equations in dq0 reference frame can be obtained.

$$\begin{cases} L_d \frac{dI_{sd}}{dt} = -RI_{sd} + \omega L_d I_{sq} - V_d + V_{sd} \\ L_d \frac{dI_{sq}}{dt} = -RI_{sq} + \omega L_d I_{sd} - V_q + V_{sq} \\ L_d \frac{dI_{s0}}{dt} = -RI_{s0} - V_0 + V_{s0} \end{cases} \quad (9)$$

$$\begin{cases} C_d \frac{dV_d}{dt} = \omega C_d V_q + I_{sd} - I_d \\ C_d \frac{dV_q}{dt} = -\omega C_d V_d + I_{sq} - I_q \\ C_d \frac{dV_0}{dt} = I_{s0} - I_0 \end{cases} \quad (10)$$

From the Eqs. (9) and (10), after dq0 transformation, the control system of the converter can be divided into two subsystems. One is coupling dq axis system which needs to be decoupled, and the other is 0 axis system. Since the injected currents (I_r, I_y, I_b) will be unbalanced under unsymmetrical fault, not only the sum of V_{dc1} and V_{dc2} a should be controlled to remain the same, but also the voltage balance control for the split DC link capacitors C1 and C2 should be considered [11].

The voltage equations of the capacitors can be shown in Eq.(11).

$$\begin{cases} V_{dc1} + V_{dc2} = V_{dc} \\ C_2 \frac{dV_{dc2}}{dt} - C_1 \frac{dV_{dc1}}{dt} = 3(I_0 + C_d \frac{dV_0}{dt}) \end{cases} \quad (11)$$

Based on Eqs. (9) – (11), the control system diagram of the three phase four-wire PWM converter is shown as Fig. 2. The double loop control strategy, consisting of voltage outer loop and current inner loop, is adopted.

From Fig. 2, it is known that the 0 axis current reference I_{s0} will be generated by the difference between the controllers of V_{dc2} and V_{dc1} . Since $V_{dc1} + V_{dc2} = V_{dc}$ will be controlled to stay the same, $C_1 \frac{dV_{dc2}}{dt} + C_2 \frac{dV_{dc1}}{dt} = 0$ can be obtained.

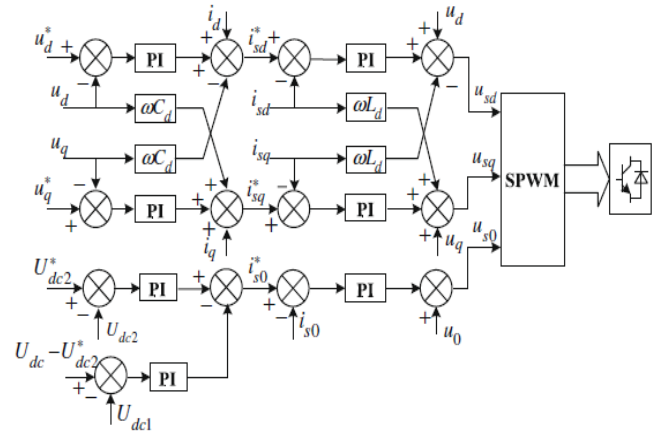


Fig- 2. Control system diagram of PWM converter.

Consequently, the variation trends of V_{dc2} and V_{dc1} will be opposite with each other, so as to keep the voltage balance of the split DC link capacitors. According to the operating state of the main circuit and the current-limiting mode of the integrated active SFCL, the current reference signals (I_r, I_y, I_b) can be known. Further, based on Eq. (5), the reference signals (V_r, V_y, V_b) will be obtained, and then the voltage reference signals of the converter (V_d, V_q, V_0) can be achieved from Eq. (12).

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos \omega t & \sin \omega t & 0 \\ -\sin \omega t & \cos \omega t & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} V_r \\ V_y \\ V_b \end{bmatrix} \quad (12)$$

As the reference signals (I_0, V_0) have been achieved, the voltage reference signal of the capacitor C2 (V_{dc2}) can be obtained from the equation $2C_2 \frac{dV_{dc2}}{dt} = 3(I_0 + C_d \frac{dV_0}{dt})$

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IV.SIMULATION EVALUATION

To verify the feasibility and validity of the presented control strategy, using MATLAB, the simulation model of the integrated active SFCL is built. The model parameters are expressed as:

$$Z_1 = (0.19 + j0.0068) \Omega, Z_2 = (15 + j0.063) \Omega,$$

$$V_{SR} = 220 \sin \omega t \quad V_{SY} = 220 \sin(\omega t - 2\pi/3) \text{ V},$$

$$V_{SB} = 220 \sin(\omega t + 2\pi/3) \text{ V}, f=50 \text{ Hz}, L_{s1}=0.7\text{mH}, L_{s2} = 0.11\text{mH}, M_s = 0.005 \text{ mH}, C_1 = C_2 = 2000 \mu\text{ F}, V_{dc} = 600 \text{ V}, L_d = 100 \text{ mH}, C_d = 1000 \mu\text{ F}.$$

Taking the single-phase and three-phase faults for examples, the performances of the converter corresponding to the current limiting mode 3, under unsymmetrical and symmetrical fault conditions are analyzed, respectively. Besides, the voltage and current reference signals of the converter under the different conditions. In the simulation model, it is set that once detecting the fundamental wave of the line current is larger than the given threshold value, the converter's input voltage reference signals will be adjusted to make the SFCL switch to the mode 3. Since the root mean-square (RMS) of the fundamental wave is about 8A in normal state.

A. Single-phase short-circuit

Supposing that the node U is grounded at $t = 0.1 \text{ s}$ and the fault angle is 0° (for phase R), Fig. 3 shows the working performances of the integrated active SFCL under this condition. After the fault happens, the phase angle of the injected current I_r can be adjusted in time by the converter, so as to make the SFCL work on the mode3, and the first peak value of the fault current I_{Rf} can be limited to 60 A.

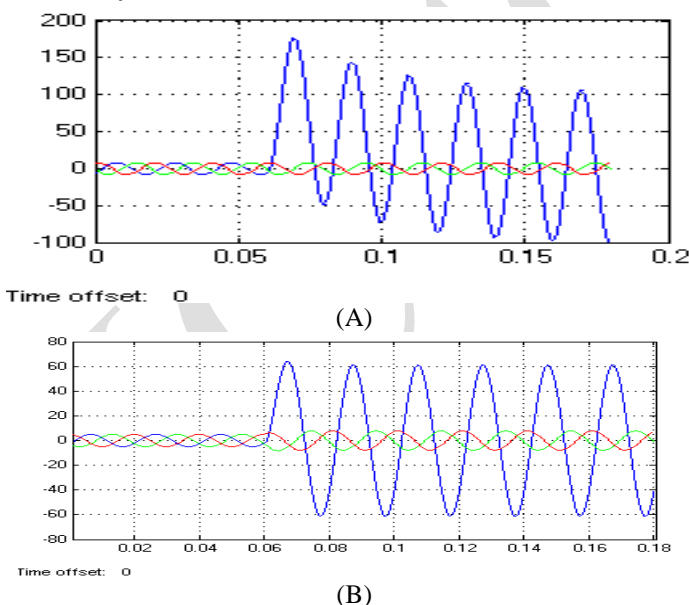


Fig-3. Line current I_R, I_Y, I_B under single phase fault. (A) Without SFCL ,(B) With SFCL.

Without the operation of SFCL, the fault current I_{Rf} will rise to 175 A. As a result, the reduction of the expected fault current is 115 A. Fig.3 shows the single phase fault current with SFCL and without SFCL. After the injected current I_r is regulated by the converter, the each capacitor voltage will be composed of two parts. One is the initial DC component, whose value is 300 V, and the total DC voltage can be kept at the level of 600 V. Fig-3 indicates that performance of voltage compensation type active SFCL under single phase fault.

B. Three phase short-circuit

Supposing that the three-phase grounded fault happens at $t = 0.1 \text{ s}$ (nodes U, V and W are all grounded). Fig. 4 shows the current-limiting characteristics of the integrated active SFCL, compared with the case of lacking SFCL. After installing the SFCL, the fault currents (I_{Rf}, I_{Yf}, I_{Bf}) can be limited to 60 A, 59 A, 58 A, respectively, in contrast with 175 A, 100 A, 90 A under the condition without SFCL. The reduction of the expected fault currents will be 115 A, 41 A, 32A, respectively. Obviously, the injected current in the each superconducting transformer's secondary winding can be regulated in time after the fault occurs. We reduce three phase fault current with the help of SFCL through converter applied voltage V_{dc1} and V_{dc2} and current I_R, I_Y, I_B , and they will maintained at minimum value.

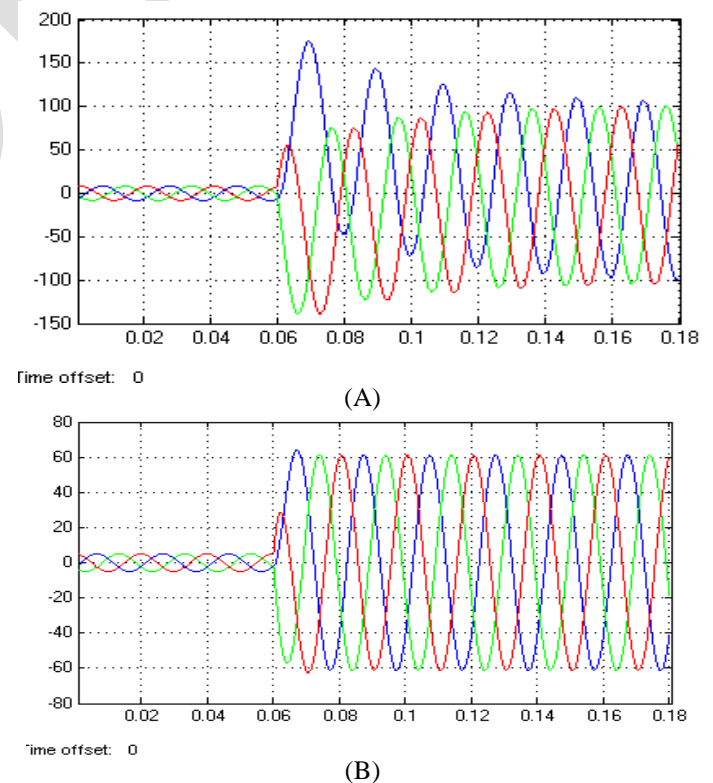


Fig-4. Line current I_R, I_Y, I_B under three phase fault. (A) Without SFCL ,(B) With SFCL.

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The harmonic distortions in the voltages occur within the first 1/2 cycle after the fault, and further they will be filtered by Ld and Cd. Through the filtering process, the total harmonic distortion (THD) of the voltages will be smaller than 1%. The different faults are calculated, and the three-phase fault can be considered as the most severe one for the integrated active SFCL. Under this condition, the injected currents (I_r, I_y, I_b) will all be adjusted by the converter, and the each superconducting transformer's primary voltage and current, as well as secondary voltage, will all rise to a certain level, respectively. Consequently, the output power of the converter and the AC losses of the integrated active SFCL under the three-phase fault will be larger than that under the other types of faults.

C. Voltage across SFCL in R-phase.

By adjusting parameter of primary winding, we can minimize voltage drop across super conducting fault current limiter. Primary winding resistance is maintained at 2.5Ω and inductance 0.7mH . In normal state voltage across SFCL is maintained at 12V, during single phase fault is happen at node U voltage drop is increased about 151V due to the increased SFCL impedance after single phase fault happen. Fig-5 indicates that voltage across SFCL in normal state and after fault is happened.

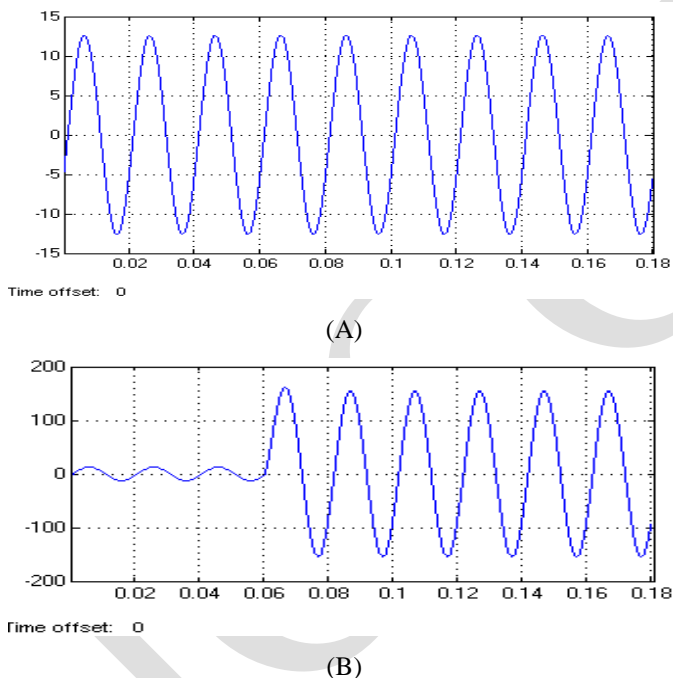


Fig -5. Voltage across SFCL (A) In Normal state, (B) Single phase fault is happen on R-phase.

V. CONCLUSION

In this paper, an active SFCL is presented to limit fault current level. Under normal operating conditions, the SFCL has no influence on main circuit. During fault conditions the extra impedance will be offered by the SFCL to main circuit to reduce fault current level. The simulation results show that using SFCL fault current level can be reduced to certain level by regulating

the amplitude and phase angle of the current in the second windings of SFCL.

REFERENCES

- [1] I.Chen, Y.J.Tang, M.Song, J.Shi, L.Ren, "Parameter design and performance simulation of a 10 kV voltage compensation type active superconducting fault current limiter," *Physica C* 494 (2013) 349-354.
- [2] J.S. Kim, S.H. Lim, J.C. Kim, "Analysis on fault current limiting and bus-voltage sag suppressing operations of SFCLs using magnetic coupling of two coils according to their application locations in a power distribution system," *Physica C* 471 (2011) 1358-1363.
- [3] S. Bacha, D. Frey, J.L. Schanen, E. Lepelleter, P.O. Jeannin, R. Caire, "Short-circuit limitation thanks to a series Connected VSC," In: *Twenty-Third Annual Applied Power Electronics Conference and Exposition*, IEEE Press, 2008, pp. 1938-1945.
- [4] T. Okawa, N.X. Tung, G. Fujita, Y. Takemoto, K. Horikoshi, "Fault Current Limiter based on Series Active Compensator," In: *Twenty-Sixth Annual Applied Power Electronics Conference and Exposition*, IEEE Press, 2011, pp. 1564-1568.
- [5] J. Shi, Y.J. Tang, C. Wang, Y.S. Zhou, J.D. Li, L. Ren, S.J. Cheng, "Active superconducting DC fault current limiter based on flux compensation," *Physica C* 442 (2006) 108-112.
- [6] L. Chen, Y.J. Tang, J. Shi, Z. Sun, "Simulations and experimental analyses of the active superconducting fault current limiter," *Physica C* 459 (2007) 27-32.
- [7] L. Chen, Y.J. Tang, J. Shi, N. Chen, M. Song, S.J. Cheng, Y. Hu, X.S. Chen, "Influence of a voltage compensation type active superconducting fault current limiter on the transient stability of power system," *Physica C* 469 (2009) 1760-1764.
- [8] L. Chen, Y.J. Tang, J. Shi, L. Ren, M. Song, S.J. Cheng, Y. Hu, X.S. Chen, "Effects of a voltage compensation type active superconducting fault current limiter on distance relay protection," *Physica C* 470 (2010) 1662-1665.
- [9] Y. Hiroshi, K. Teruo, "Stability Analysis of Air-Core Superconducting Power Transformer," *IEEE Trans. Applied Superconducting*, 7 (1997) 1013-1016.
- [10] Y. Hiroshi, M. Hajime, S. Yukihiro, K. Teruo, "Magnetic field analysis of Air-Core Superconducting transformer," *IEEE Trans. Magn.* 31 (1995) 4124 - 4126.
- [11] L. Chen, Y.J. Tang, J. Shi, Z. Li, L. Ren, S.J. Cheng, "Control strategy for three-phase four-wire PWM converter of integrated voltage compensation type active SFCL," *Physica C* 470 (2010) 231-235.
- [12] M. Song, Y. Tang, J. Li, Y. Zhou, L. Chen, L. Ren, "Thermal analysis of HTS air-core transformer used in voltage compensation type active SFCL," *Physica C* 470 (2010) 1657-1661.